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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,762	12/29/2000	Sailesh Kottapalli	2207/10121	5066

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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/751,762	KOTTAPALLI ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1- 21 are presented for examination.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reasons are given below.

As to claim 1,5, the practical application for determining the if the stalled is due to the loading of memory and flushing the instruction after the predetermined number of cycles if data is to be loaded from the memory before execution is not clear. Furthermore, determining the stall due to memory loading and the flushing of the instruction after a number of cycles if data is to be loaded from the memory is an intended result, not a positive recitation of the claim scope. The focus in not on the step taken to achieve a final result which is useful, tangible, and concrete, but rather the final result achieved which is useful, tangible, and concrete (see MPEP 2100). No final result can be found for the flushing of the instructions. Therefore, it is directed to a non-statutory subject matter.

As to claim 10, the structural components the of the schedule to impart the functionality of the processing system are not being recited into the claim, and the pipeline control logic is an abstract idea.

As to claim 16, although claim 16 additionally recited the memory coupled to a bus, and the processing system coupled to memory, it is read as a general arrangement of the elements, and it does not present any final result which is useful, tangible, and concrete.

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claim 1, rejected under 35 U.S.C. 102(a) as being anticipated by Gottlieb (6,016,542).

As to claim 1, Gottlieb taught at least :

a) determining if stall is due to loading of data from memory (see stall due to loading of data from memory in col.3, lines 24-30, lines 61-65, col.6, lines 42-67);

b) flushing an instruction from a thread in a pipeline of the processing system after a predetermined number of cycles if data is to be loaded from the memory before executing the instruction (see 30 cycles required flush of instructions in a pipeline as a thread switch condition in col.2,lines 54-61, see the thread switch condition after the detection of the stall in col.7, lines 13-26, see background teaching in col.1, lines 45-55).

Gottlieb taught a switching condition after detection of pipeline stall due to the memory load (see col.7, lines 13-26). Gottlieb also taught a flush of instructions that required

30 cycles as a switching condition (see col.2, lines 54-64). Therefore, Gottlieb taught the flush of the instructions in the pipeline after a number of cycles if the data is to be loaded form memory.

2.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Eikemeyer (6,694,425).

4. As to claims 1,5, 10 , 16, Eikemeyer taught a pipeline system comprising at least :

a) determining if a stalled operation of a first thread is due to a loading of data from a memory device (see the stalled thread in dispatch stage in col.1, lines 6-12, see also the stall detector in col.6, lines 15-18 , col.8, lines 35-38, see load /store instruction in col.3, lines 40-44, see also the reasons for stalling for the loading of data from memory in col.10, lines 35-45); and

b) flushing an instruction from the thread a pipeline of said processing system

after a predetermined number of cycles if data is to loaded from memory device before executing the instruction (see the flushing of the instruction of the thread in col.1, lines 6-12, see also the flushing of the instruction in the pipeline in col.6, lines 18-26, col.11, lines 41-49).

Applicant stated in the remark that waiting for fetch or decode the stalled thread until a predetermined number of cycles have been passed is not the same as flushing an instruction from the memory after a predetermined number of cycles if data is to be loaded from the memory. Applicant is directed to before and during a flush.

As to remark above, the question is what that "predetermined number of cycles" is, this number of cycles are the delay of the memory cache miss (see applicant's page 5, lines 1-16). Eikemeyer also taught his predetermined number of cycles were due to the cache miss (see col.13, lines 5-9).

As to before, after, or during a flush, applicant never recite before, after, or during a flush.

Nevertheless, Eikemeyer 's flush was directed to before and during the flush (the restarting of thread (see the refrain for the thread again until the predetermined number of cycles has passed). Eikwmeyer clearly taught that should the thread again encounter the dispatch block(e.g. due to cache miss, see col.13, lines 5-15), the dispatch flush can occur again. So the instruction flush was before the number of predetermined number of cycles. See also the restart of flush after a number of cycles has been passed in col.5, lines 26-31.

5. As to claim 5, Eikemeyer also taught the a predetermined cycles before execution (see col.13, lines 5-15, see also the delay cycles before restarting the instruction in col.5, lines 26-30).

6. As to claims 2, 6, Eikemeyer also taught a system memory (see system memory in col.8, lines 55-66).

7. As to claims 3, 7,11, 17, Eikemeyer also taught cache miss (see cache miss in col.3, lines 40-44, col.13, lines 5-8). No explicitly explicitly teaching of cache missing marking has been shown, but Eikimeyer taught cache miss as reason for stalling (see col.3, lines 40-44), therefore, it must have cache miss marking, otherwise, it would not have known which instruction was staling.

8. As to claims 4,8, Eikemeyer also taught rescheduling of instruction (see the reflect and reenter of the flushed instruction in col.12, lines 58-67, col.13, lines 1-15, see also the delay cycles before restarting the instruction in col.5, lines 26-30).

9. As to claim 9, see the delay cycles before restarting the instruction in col.5lines 26-30, see the reenter into the normal pipeline in col.12, lines 58-67, col.13 , lines 1-15, see , see also the execution after the dispatch in col.10, lines 20-26).

10. As to claims 12,13,18, 19, see the exception in col.3, lines 26-35, 36-44, col.10, lines 35-42 for reasons for stalling. See also the determination of the older instructions

in col.12, lines 42-63. No explicitly teaching of cache missing marking has been shown, but Eikimeyer taught cache miss as reason for stalling (see col.3, lines 40-44), therefore, it must have cache miss marking, otherwise, it would not have known which instruction was staling.

11. As to claims 15,21, see the data available in col.3, lines 40-44. See also the reentering to normal pipeline in col.13, lines 1-15.

12. As to claim 20, see fetch unit 270 in fig.2A.

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Panwar et al. (5,890,008) is cited for the known teaching of the flushing of instructions on exception and the retirement of the instructions (se col.13, lines 36-67).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

PRIMARY EXAMINER